REMARKS

This responds to the Office Action mailed on July 26, 2006. In this response, claims 1, 10, and 31 are amended. Claim 16 was canceled and no claims were added. As a result, claims 1-15, 17-20, and 28-33 are now pending in this application. Reconsideration of this application in view of the above amendments and the following remarks is respectfully requested.

Objection of the Claims

Objection: Claim 31 was objected to as being unclear. According to the Examiner, lines 1-2 are unclear. The phrase of "the test device is a pad on one of the first and second surfaces" is not understood because as disclosed in a specification, the test device (550), see paragraph [0030] includes probes (554) and test electronic (556), so the test device is an external test equipment to test components (for example, pad, component, chip or circuitries, etc.) on a circuit board and not belongs to the PCB (the pad is formed on the PCB). Therefore, the test device is not a pad.

The examiner assumed the test device and a probe.

Response: The claim was corrected to overcome the objection set forth by the Examiner. Claim 31 now recites that the test device includes a pad so as to clearly state the nature of the invention and overcome the objection.

The Applicant objects to the Examiner's assumption and requests that the Examiner produce art in support of any rejections.

§103 Rejection of the Claims

A. Rejection: Claims 1-9 and 28-33 were rejected under 35 USC § 103(a) as being unpatentable over Shiraki (U.S. 6,969,808) in view of Ott et al. (U.S. 6,147,505).

B. Response: In order for the Examiner to establish a prima facie case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the

references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference or references must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. M.P.E.P. § 2142 (citing In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir. 1991)).

Claim 1 recites "...a signal carrying plated through hole terminating at the at least one of the first major surface and the second major exterior surface; a pad between the first major surface and the second major surface, the signal carrying plated through hole connected to the pad; an antipad element substantially surrounding the pad; a plane metallization layer substantially surrounding the pad and the antipad; a plated through hole attached to the plane metallization layer and terminating at the at least one of the first major exterior surface and the second major exterior surface ... and a circuit tester for determining if a current will flow between the pad and the signal carrying via, and the plane metallization layer to test the spacing of a plane metallization layer from a signal through hole that passes through the plane metallization layer." The combination of Shiraki (U.S. 6,969,808) and Ott et al. (U.S. 6,147,505) fails to teach or suggest the all of the claim elements needed to make the claimed combination recited in claim 1. Shiraki does not include the pad connected to the signal carrying via and does not appear to teach or show a plane metallization layer that substantially surrounds the pad and the antipad. Ott et al. does not include these elements since it is directed to an adapter for electrically testing a printed circuit board.

In addition to not teaching or suggesting all the elements, one of ordinary skill in the art would not combine Shiraki with Ott et al. since doing so would destroy the Shiraki reference. One of the objects of the arrangement of ground through holes and signal through holes in the Shiraki invention "...is to provide a multi-layer printed circuit board which can improve impedance matching even in case of a high signal frequency." (See column 2, lines 6-9 of Shiraki). The specification of the Shiraki reference further details how impedance matching is achieved in the following:

> "A signal transmitted through signal line 11 and reflected in through-hole 21, is transmitted to ground through-hole 41 most adjacent to through-hole 21 via land 31 electrically connected to through-hole 21, as shown with a dotted arrow in FIG. 4. The transmission is implemented by capacitive coupling depending on capacitance between a portion of the land 31 opposite to ground through-hole 41 and the ground through-hole. As in the present embodiment, the portion of land 31 opposite to ground through-hole 41 most adjacent to center C of land 31 is cut away to form the portion of the shorter radius 33. Consequently, land 31 of through-hole 21 and ground through-hole 41 can be spaced further apart to provide reduced capacitance. As a result, a resonance frequency can be increased to improve impedance matching to accommodate a signal of higher frequency.
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> Additionally, in the present embodiment, ground through-holes 41 are positioned in upward and downward directions of land 31 of through-hole 21 in FIG. 7, i.e., in a direction perpendicular to that of signal line 11 with center C of land 31 defined as a reference point. Therefore, a portion of land 31 to be cut away is 90 degree offset from a connection of signal line 11 and land 31. Thus, an original function of land 31 to ensure conduction even if through-hole 21 has a somewhat offset position, is less impaired. Additionally, in the present embodiment, the portion of the minimum radius 34 in the portion of the shorter radius 33 of land 31 of through-holes 21 corresponds to a portion opposite to ground through-hole 41. Therefore, impedance matching can be improved more effectively." (See column 2, line 53 to column 3, line 14 of Shiraki).

Thus, the ground vias are positioned to improve impedance matching for signal lines and signal vias that carry high frequency signals. Applying a testing apparatus to determine if current will flow between a signal line and a ground line will destroy improvements in impedance matching since a voltage will be applied between the various vias. Therefore, one of ordinary skill would not combine these two references since doing so would destroy one of the stated objects of the Shiraki invention. The destruction of the Shiraki reference is evidence that there is no reason to combine the Shiraki and the Ott references.

It should also be noted that Shiraki is unconcerned about testing. Shiraki fails to discuss any kind of testing or testing apparatus. Simply stating that one would combine Shiraki with Ott (an adapter for testing printed circuit boards) seems to be using the application as a blueprint for the combination of references. This is improper.

For all of the above stated reasons, claim 1 now overcomes the Examiner's rejection under 35 USC § 103(a) as being unpatentable over Shiraki (U.S. 6,969,808) in view of Ott et al. (U.S. 6,147,505). Claims 2-9 depend from claim 1 and include the recitations of claim 1 by their

dependency. Accordingly, claims 2-9 now also overcome the Examiner's rejection under 35 USC § 103(a) as being unpatentable over Shiraki (U.S. 6,969,808) in view of Ott et al. (U.S. 6,147,505).

In rejecting claims 28-33, the Examiner contends that "It would have been obvious to one of ordinary skill in the art a the time the invention was made to have a teaching of Ott et al. employed in the device of Shiraki in order to prevent a short circuit." Ott et al. teaches a testing apparatus with a number of probes and a testing nest that holds a printed circuit board. It is doubtful one would have added the Ott et al. hardware to Shiraki in order to prevent a short circuit. The result would be an unusually large and cumbersome device that could not be used in an electronics world that constantly requires more capability out of smaller packages. Enlarging a package would not be a real option.

Claim 28 recites "...a plated through hole attached to a plane metallization layer and terminating at the at least one of the first major exterior surface and the second major exterior surface including a plurality of component mounting pads, the plated through hole attached to the plane metallization layer within the device, and electrically isolated from the plurality of component mounting pads, wherein the feature positioned within the device passes through the plane metallization layer and is isolated from the plane metallization layer; and a test device electrically coupled to the feature for testing the spacing between the feature and the plane metallization layer." The Shiraki reference is directed to an arrangement of vias surrounding the signal feature and the signal via for improving impedance matching. There is no teaching or suggestion of testing. Adding the testing apparatus of Ott et al. to the Shiraki reference would destroy the impedance matching aspect of Shiraki. In addition, Ott et al. is not concerned with testing the spacing between a feature and a plane metallization layer. Accordingly, a proper *prima facie* case of obviousness has not been made with respect to claim 28 and the claims dependent on that claim, namely claims 29-33.

C. Rejection: Claims 10-15 were rejected under 35 USC § 103(a) as being unpatentable over Shiraki (U.S. 6,969,808) in view of Conn et al. (U.S. 5,418,690).

D. Response: Claim 10, as now amended, recites "...a signal carrying plated through hole terminating at the at least one of the first major surface and the second major exterior surface; a pad between the first major surface and the second major surface, the signal carrying plated through hole connected to the pad; an antipad element substantially surrounding the pad; a plane metallization layer substantially surrounding the pad and antipad within the device; and a plated through hole attached to the plane metallization layer and terminating at the at least one of the first major exterior surface and the second major exterior surface including the plurality of component mounting pads, the plated through hole attached to the plane metallization layer electrically isolated from the plurality of component mounting pads; and a circuit test apparatus for testing the spacing between the plane metallization layer and the pad associated with the signal carrying through hole, the circuit test apparatus under the control of the processor." Claim 10 now has a structure similar to claim 1 which is not found in either the Shiraki reference or the Conn et al reference. In other words, neither reference teaches or suggests the pad connected to the signal carrying via or the plane metallization layer that substantially surrounds the pad and the antipad. In addition, neither reference teaches or suggests the circuit test apparatus or a circuit test apparatus under control of a processor. Since the prior art reference or references fail to teach or suggest all the claim limitations now found in claim 10, the claim now overcomes the Examiner's rejection under 35 USC § 103(a) as being unpatentable over Shiraki (U.S. 6,969,808) in view of Conn et al. (U.S. 5,418,690). Claims 11-15 depend from claim 10 and overcome the rejection for the same reasons set forth above.

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E. Rejection: Claim 16 was rejected under 35 USC § 103(a) as being unpatentable over Shiraki (U.S. 6,969,808) in view of Conn et al. (U.S. 5,418,690) and further in view of Ott et al. (U.S. 6,147,505).

F. Response: By this response, claim 16 has been canceled thereby obviating this rejection.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6977 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Signature